In the Specification

Applicant presents replacement and amended paragraphs below indicating the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

On page 1 before line 2 please insert the heading as follows:

Field of the Invention

On page 1, before line 6 please insert the heading as follows:

Background of the Invention

Please amend the paragraph beginning at page 3, line 10 as follows:

VHDL supports many abstract data types which are used to ~~described~~ describe different signal strengths or commonly used simulation conditions such as unknowns and high-impedance conditions. These non-standard data types have been adopted by the IEEE as standard 1164. Such data types are not applicable to analog simulators which require true analog signals rather than abstract data types.

On page 3, before line 17 please insert the heading as follows:

Summary of the Invention

Please amend the paragraph beginning at page 3, line 21 as follows:

According to a first aspect of the present invention there is provided a method of identifying an inaccurate model of a hardware circuit comprising the steps of simulating the model of the circuit by applying a plurality of signals, said plurality of signals having at least one abstract data type level ~~are~~ to provide a set of expected results; replacing the ~~or each~~ at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model; resimulating the model with said expanded set; and comparing the two sets of results and providing an output signal indicating if the model is inaccurate if the results contradict.

Please amend the paragraph beginning at page 4, line 18 as follows:

According to a second aspect of the present invention, there is provided a system for identifying an inaccurate model of a hardware circuit comprising means for simulating the model of the circuit by applying a plurality of signals, said plurality of signals having at least one abstract data type level to provide a set of expected results; means for replacing the ~~or each~~ at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model; means for resimulating the model with said expanded set; means for comparing the two sets of results and providing an output signal indicating if the model is inaccurate if the results contradict.

On page 4, before line 31 please insert the heading as follows:

Description of the Drawings

Please amend the paragraph beginning at page 4, line 35 as follows:

Figure 2 illustrates an inverter logic gate as ~~modelled~~ modeled by an analog model;

On page 5, before line 7 please insert the heading as follows:

Detailed Description

Please amend the paragraph beginning at page 7, line 17 as follows:

'H' : This is exactly the same as an 'L' however in the opposite sense, that is to say it represents a weak high.

Please amend the paragraph beginning at page 10, line 12 as follows:

Embodiments of the present invention use WIF files. A WIF (waveform interface format) file is an ASCII based file which contains information needed to describe the model's interface (names of ports, directions of signals – input/output/bi-directional, and types of signals) and signal activity against time in a tabular format. In embodiments of the present invention, the IEEE 9 logic states discussed previously are used to indicate both driven and driving states. The pin

direction is then used to determine what needs to be done to either drive the value or test for the existence of a value in one of the many supported simulators. Additional parameters can be ~~spec5ified~~ specified using specially defined comments. These are then used to alter the behaviour of the tool and the simulations/interpretations performed by the tool.

Please amend the paragraph beginning at page 12, line 28 as follows:

The third stage takes place after the ELDO simulation is carried out using the expanded logic package and the results are verified against the expected reference results from the VHDL simulation. Not only can the tool check that the outputs match but further verifications can be made to the results to find potential bad transitions.